Patent claims

1. An integrated circuit comprising a multiplicity of logic gates (2) for implementing a logic function of the integrated circuit (1), and a self-test circuit (3) for performing an internal self test of the multiplicity of logic gates (2), the self-test circuit (3) exhibiting a test pattern generator (4) for generating a test pattern (16), a test response analyzer (5) for evaluating a test response (17) and an input/output circuit (7) by means of which the self-test circuit (3) performs a logic test of an external circuit (14, 15), characterized in that the multiplicity of logic gates (2) and the external circuit (14, 15; 23) are tested at the same time, a first part (TM1) of the test pattern (16) being supplied to the multiplicity of logic gates (2) and a second part (TM2) being supplied to the external circuit (14, 15; 23) via the input/output circuit (7) whereas the test response (17) is produced from a first part of response signals (TA1) of the multiplicity of logic gates (2) and from a second part of response signals (TA2) of the external logic circuit (14, 15; 23).

2. The integrated circuit as claimed in claim 1, characterized in that the test pattern generator (4) and the test response analyzer (5) consist of linear-feedback shift registers.

3. The integrated circuit as claimed in claim 1 or 2, characterized in that

the test pattern generator (4) generates pseudo-random vectors as test pattern.

4. The integrated circuit as claimed in one of claims 1 to 3, characterized in that the input/output circuit (7) exhibits input/output drivers (9, 9') for sending and receiving unidirectional signals (10, 11) between the self-test circuit (3) and the external circuit (14).

5. The integrated circuit as claimed in one of claims 1 to 4, characterized in that the input/output circuit (7) exhibits controllable input/output drivers (8) for sending and receiving bidirectional signals (12) between the self-test circuit (3) and the external circuit (15), a control device (6) controlling the drivers of the output circuit (7) and of the external circuit (15).

6. The integrated circuit as claimed in claim 5, characterized in that the control device (6) controls the self-test circuit (3) and the output circuit (7) in such a manner that an initialization of the external circuit (15; 23) is performed in a first test cycle and the self test of the multiplicity of logic gates (2) and of the external circuit (15) is performed in a second test cycle.

7. The integrated circuit as claimed in claim 5 or 6, characterized in that

the input/output circuit (7) exhibits a bus connection for connecting to an external bus structure (12') and the control device exhibits a bus control (6'), external circuit elements (23) connected to the bus structure (12') being selectively selected for a self test via respective enable signals (13').

8. The integrated circuit as claimed in claim 7, characterized in that the bus control (6') exhibits a counter for counting a bus clock signal, the controllable output drivers (8) only being selected during all even-numbered clock cycles of the bus clock signal and the respective enable signals (13') being output sequentially during all odd-numbered clock cycles of the bus clock signal for enabling the respective external circuit elements (23).

9. The integrated circuit as claimed in one of claims 1 to 8, characterized in that the input/output circuit (7) can be selectively deactivated.

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